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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,996	07/26/2000	R. Dean Adams	FIS9-2000-0138US1	8495

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EXAMINER

CHAUDRY, MUJTABA M

ART UNIT	PAPER NUMBER
2133	15

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/625,996	ADAMS ET AL.
	Examiner	Art Unit
	Mujtaba K Chaudry	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 June 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-17 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect to currently amended claims 1 and 8, previously amended claim 12 and original claims 2-7, 9-11 and 13-17 have been fully considered but are not persuasive. Examiner has provided with numerous issues that need to be addressed in the claims' language.

Claim Rejections - 35 USC § 112

Claim 1, 8, 12 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 8, 12 and 17 may include similar limitations that are also addressed herein below.

- Claim 1 recites in part, "...a built-in self-test arrangement..." which is not clear. Applicant is suggested to link the BIST arrangement with the actual integrated circuit and explicitly state that in the claim language.
- Applicant uses the term "means" throughout the claim language excessively and is causing the claim to fall apart. For example, it is not clear if the "means for discriminating a source of test command" is included within the "means for storing test instruction" or in the integrated circuit.
- Throughout the claims Applicant uses terms "test command" and "test instruction." It is not clear if these are one of the same, and if so they should be written in such a way to

avoid antecedent problems. Again, the test command/instruction does not link with the device. Applicant needs to incorporate how the test commands/instructions are communicated.

- The claims recite in part, “performing manufacturing level and board level testing.” Examiner is not sure how two tests can possibly be performed at one time when one is suppose to be before the other. In other words the manufacturing level test is done before the circuit is made and the board level testing is done when circuit is made. The Examiner would like to point out that, it seems as though Applicant intended the limitation to recite, “performing manufacturing level **or** board level testing.”

Appropriate corrections are required.

Response to Arguments

Applicant contends, “...in Schwartz testing is always initiated by debugging signal and no different levels of testing is distinguished.” The Examiner disagrees. The Examiner would like to point out that Schwartz teaches (col. 1, lines 5-40) to provide adjustable tests for integrated circuits. Furthermore, Schwartz teaches (col. 1, lines 10-25) to test integrated circuits at the manufacture level and by external tester (ATE—automatic test generator). Schwartz teaches the use of built-in self-test (BIST) circuitry wherein additional hardware is added to a design so that testing is accomplished with a reduced need for external special purpose testing hardware. For example, when BIST circuitry uses a pseudorandom vector generator and a data compactor. The generator produces the test vectors to be applied to a circuit under test and the compactor reduces the response to these vectors to a single value known as the signature. It is

then possible for the ATE to initialize or provide parameters to the generator and examine signatures from the compactor to verify the functionality of the chip.

Applicant contends, "...manufacturing level, board level and system level is not shown..." The Examiner disagrees in view of the above stated reasons and further elaborates. Schwartz teaches (col. 2, lines 1-14) the debug signal which when is de-asserted the system level test information from the BIST is used to test the embedded device. Whereas when the debug signal is asserted the external test information is used to test the embedded device. Specifically, Schwartz teaches that when the debug signal is asserted, the multiplexer forwards external data from the user to the embedded device, thereby allowing the user to execute **customized tests** on the embedded device.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Applicant states, "It should be noted that all means structures are located within the BIST.") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, the Examiner would like to point out that even if all the means structures—if claimed—are stored in the BIST structure then the claim would essentially be claim a BIST structure which is well known in the art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-17 are rejected under 35 U.S.C. 102(e) as being unpatentable over Schwartz (USPN 5982681). See paper No. 7.

The Examiner disagrees with the Applicant and maintains all rejections of currently amended claims 1 and 8, previously amended claim 12 and original claims 2-7, 9-11 and 13-17. All arguments have been considered. It is the Examiner's conclusion that currently amended claims 1 and 8, previously amended claim 12 and original claims 2-7, 9-11 and 13-17 are not patentably distinct or non-obvious over the prior art of record.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schwarz teaches a method and apparatus for a reconfigurable built-in self-test circuit, which is on an integrated circuit with embedded memory. Schwarz clearly anticipates all the

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limitations stated in the present application. Applicant is further invited to visit additional prior art included in this action.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.


Mujtaba Chaudry
Art Unit 2133
June 24, 2003


ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100